REMARKS

Reconsideration of this application is respectfully requested.

Claims 1-6 and 8-14 are pending. Claims 1-6 and 8-14 stand rejected.

Claims 1 and 13 have been amended in support of the Specification. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Rejections - 35 U.S.C. §103

Claims 1 and 8-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris"). Claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris as applied to claims 1 and 8-12 above, and further in view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi"). Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris as applied to claims 1 and 8-12 above, and further in view of U.S. Patent No. 6,057,582 of Choi ("Choi_1"). Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris in view of Takeuchi as applied to claim 2 above, and further in view of Choi_1. Claims 5 and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris as applied to claims 1 and 8-12 above, and further in view of U.S. Patent No. 5, 793,088 of Choi ("Choi_2"). Claim 13 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris in view of U.S. Patent No. 6,274,894 B1 of Wieczorek, et al. ("Wieczorek") and further in view of Takeuchi. Claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gualandris in view of Wieczorek in view of Takeuchi as applied to claim 13 above, and further in view of Choi_1. The Examiner stated that

> Gualandris does not disclose an inflection point which occurs between 50-250 A laterally beneath said gate electrode and at a depth of between 12-200 A beneath said

gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these depths in order to form an adequate channel underneath the gate electrode, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

(p. 2-3, Office Action 6/11/04)

Applicants respectfully disagree. It is respectfully submitted that the cited references fail to teach or render obvious applicants' invention as set forth in claims 1-14. With respect to claim 1, applicants teach and claim a device, wherein source/drain regions have inflection points directly beneath the lower portion of the gate electrode to extend the source/drain regions the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, wherein the source and drain regions define a channel region, which is larger directly beneath the gate dielectric than between the inflection points to achieve larger channel length during the "off" state and a smaller channel length during "on" state (see Specification, pages 9-10).

Claim 1 reads as follows:

A device comprising:
a gate dielectric formed on first conductivity region of a substrate;
a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and
a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode creating inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric and define a channel region directly beneath said lower portion of said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said lower portion of said gate electrode is larger than said channel region between said inflection points.

(Claim 1) (emphasis added)

The Examiner noted that Gualandris fails to disclose the limitation of claim 1 of an inflection point, which occurs between 50-250A laterally beneath the gate electrode and at a depth of between 25-200A beneath the gate dielectric. In fact, Gualandris also fails to disclose, teach, or suggest the limitations of claim 1 of source/drain regions having inflection points directly beneath the lower portion of the gate electrode to extend the source/drain regions the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, wherein the source and drain regions define a channel region, which is larger directly beneath the gate dielectric than between the inflection points to achieve larger channel length during the "off" state and a smaller channel length during "on" state.

Gualandris, in contrast, discloses a transistor, wherein the drain/source area ("multiplication zone") is moved away from the channel region of the transistor to the distance at least several times the mean free path of the carriers, to reduce the corner and pinch effects of the transistor that are known as "gated-diode" behavior. More specifically, the source and drain areas are moved away from the channel zone down from the surface to the distance at least larger than 500Å(" 50nm") (col.2, lines 50-62; col.3, lines 3-16). To further move away the source/drain areas from the channel region, Gualandris discloses rounding the bottom corner of the excavation produced in the silicon (col 4, lines 40-50), i.e. rounded bottom corner of the source/drain regions of Gualandris does not define a channel region. To move away the drain/source area ("multiplication zone") from the channel region,

Gualandris discloses etching the silicon substrate down from the surface and then using an ion implantation to form the drain/source regions (col.5, lines 33-42).

Thus, Gualandris merely discloses conventional source and drain regions created by ion implantation in the areas of silicon substrate, which are lowered relative to the gate oxide, wherein rounding the bottom corner of the excavation produced in the silicon only further increases the distance between the drain/source areas ("multiplication zone") and the channel zone.

It is respectfully submitted that Gualandris does not disclose, teach, or suggest optimization of a transistor, as the Examiner suggested, to have an inflection point between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100 Å beneath the gate dielectric.

It would be impermissible hindsight, based on applicants' own disclosure, to make such optimization on the transistor of Gualandris.

It is respectfully submitted that Gualandris teaches away from such optimization suggested by the Examiner. In contrast to such optimization, Gualandris discloses that at distances smaller than 500 Å ("50nm") the beneficial effects of the transistor are substantially lost (col.2, lines 50-62).

Furthermore, it is respectfully submitted that if the transistor of Gualandris were optimized as the Examiner suggested, to have an inflection point between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, such an optimization would destroy the intent, purpose, and function of the transistor of Gualandris having the source/drain area moved away from the channel region to the distance at least greater than 500Å ("50nm") to reduce the corner and pinch effects.

Gualandris further teaches away from such optimization suggested by the Examiner by using a conventional ion implantation technique to form the drain/source regions, wherein wafer is exposed to the ion beam through varying angles in correspondence of the bottom corner of the depressions produced by etching in the silicon and also to some measure on the vertical walls of the etched depressions of the silicon substrate. As well known in the art of transistor fabrication, implanted impurities are introduced into the substrate with minimal lateral distribution that represents a fundamental limiting factor in fabricating some minimum sized device structures, such as the electrical channel length between source and drain in self-aligned MOS structures. Contrary to the Examiner's assertion, it is applicants' understanding that one of ordinary skill in the art would not use ion implantation to extend the source/drain regions the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, wherein the source and drain regions define a channel region, which is larger directly beneath the gate dielectric than between the inflection points, as recited in claim 1, to achieve larger channel length during the "off" state and a smaller channel length during "on" state.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. §103(a) over Gualandris.

Given that claims 2-6 and 8-12 depend, directly or indirectly, on claim 1 and add additional limitations, applicants respectfully submit that claims 2-12 are likewise not obvious under 35 U.S.C. §103(a) over Gualandris.

Because claim 13 contains at least the same limitations as claim 1, applicants respectfully submit that claim 13 is likewise not obvious under 35 U.S.C. §103(a) over Gualandris.

Given that claim 14 depends directly on claim 13 and add additional limitations, applicants respectfully submit that claim 14 is likewise not obvious under 35 U.S.C. §103(a) over Gualandris.

Similarly to Gualandris, neither Gualandris, Takeuchi, Choi_1, Choi_2, nor Wieczorek discloses, teaches, or suggests the limitations of claim 1 of source/drain regions having inflection points directly beneath the lower portion of the gate electrode to extend the source/drain regions the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, wherein the source and drain regions define a channel region, which is larger directly beneath the gate dielectric than between the inflection points to achieve larger channel length during the "off" state and a smaller channel length during "on" state.

In fact, Takeuchi discloses elevated drain/source regions of the transistor formed from a thin semiconductor film layer of the appropriate conductivity type on the surface of the substrate with the source and drain junctions having minimal extensions into the substrate, only beneath the vertical sidewall isolators of the gate electrode, aiming at the ideal junction depth of zero.

Choi_1, in contrast, discloses a transistor having the gate electrode with center portions formed thicker than the end portions and conventional drain/source regions formed on both sides, and not underneath, the gate electrode.

Choi_2, in contrast, discloses forming source/drain regions on both sides of the gate electrode, underneath isolating sidewalls, and not underneath the gate electrode.

Wieczorek, unlike the presently claimed subject matter, discloses a transistor with source and drain regions having lower-bandgap portions that underlie sidewall spacers of the

gate electrode and not the gate electrode itself (see, for example, Fig. 10). Moreover, citing prior art, Wieczorek points out that extending the source/drain regions underneath the gate electrode is undesirable.

Hence, none of the references cited by the Examiner discloses, teaches, or suggests the limitations of claim 1 of source/drain regions having inflection points directly beneath the lower portion of the gate electrode to extend the source/drain regions the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, wherein the source and drain regions define a channel region, which is larger directly beneath the gate dielectric than between the inflection points to achieve larger channel length during the "off" state and a smaller channel length during "on" state.

Consequently, even if Gualandris, Takeuchi, Choi_1, Choi_2, and Wieczorek were combined, such a combination would lack such limitations of claim 1.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103 (a) over Gualandris, in view of Takeuchi, in view of Choi_1, in view of Choi_2, and further in view of Wieczorek.

Given that claims 2-6 and 8-12 depend on claim 1, either directly or indirectly, and add additional limitations, applicants respectfully submit that claims 2-6 and 8-12 are not obvious under 35 U.S.C. §103 (a) over Gualandris, in view of Takeuchi, in view of Choi_1, in view of Choi_2, and further in view of Wieczorek.

Because claim 13 contains at least the same limitations as claim 1, applicants respectfully submit that claim 13 is likewise not obvious under 35 U.S.C. §103(a) over Gualandris, in view of Takeuchi, in view of Choi_1, in view of Choi_2, and further in view of Wieczorek.

Given that claim 14 depends directly on claim 13 and add additional limitations, applicants respectfully submit that claim 14 is likewise not obvious under 35 U.S.C. §103(a) over Gualandris, in view of Takeuchi, in view of Choi_1, in view of Choi_2, and further in view of Wieczorek.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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